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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 12/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,851	CHONG, FAY	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,12-14,17-26,29-34 and 37-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,9,18,19,30,31,38 and 39* is/are allowed.

6)☒ Claim(s) *1-7,12-14,17,20-26,29,32-34 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 8,9,18,19,30,31,38,39 are allowed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6,12-14,20-26,32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito (USPN 6694475B1) in view of Bains (USPN 5701438A). As per claim 1, Saito discloses a functional unit configured to perform an operation on one or more block operands; an accumulator memory comprising a first memory bank having a first interface and a second memory bank having a second interface, wherein the first and second interfaces are independent of each other; and a control unit configured to receive a first command to perform the operation on a first operand identified by an address of the accumulator memory and to store a first result of the operation to the same address; wherein in response to receiving the first command, the control unit is configured to cause the first memory bank to output the first operand to the functional unit via the first interface and to cause the second memory bank to store the first result generated by the functional unit via the second interface in column 9, lines 1-51. The

functional unit is the XOR gate (35), the accumulator memory is RAM(p1) and RAM(p2), and the control unit is the control circuit (34).

Saito discloses wherein the functional unit is configured to perform the operation on two operands, wherein one of the operands is provided by either the first or the second memory bank and the other operand is provided by a source other than the first and second memory banks in column 9, lines 29-38.

Saito fails to explicitly state the source and the accumulator memory each comprise a same type and speed of memory.

Bains discloses this limitation in column 7, lines 35-46.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source and the accumulator memory each comprise a same type and speed of memory. A person of ordinary skill in the art would have been motivated to have the source and the accumulator memory each comprise a same type and speed of memory because the data can be accessed at the same rate so as not to reduce the overall performance of the computer system. Bains discloses this in column 1, lines 11-17.

4. As per claim 2, Saito discloses wherein in response to the functional unit completing the first operation, the control unit is configured to cause the second memory bank to provide a third operand if the control unit receives a second command that identifies the third operand using the address in column 9, lines 21-51.

5. As per claim 3, Saito discloses wherein the control unit is further configured to receive a second command to perform the operation on a third operand and to store a

second result of the operation to the address, wherein in response to receiving the second command, the control unit is configured to cause the second memory bank to provide the third operand to the functional unit via the second interface and to cause the first memory bank to store the second result via the first interface in column 9, lines 21-51.

6. As per claim 4, Saito discloses wherein in response to the functional unit completing the second operation, the control unit is configured to cause the first memory bank to provide a fourth operand if the control unit receives a third command that identifies the fourth operand using the address in column 9, lines 21-51.

7. As per claim 5, Saito discloses wherein the operation has a duration extending from when the operation is initiated to when the operation completes, and wherein for the duration of the operation that is performed on the first operand, the first memory bank is in a providing mode and the second memory bank is in a storing mode in column 9, lines 21-51.

8. As per claim 6, Saito discloses wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller in column 8, lines 11-41.

9. As per claim 10, Saito discloses wherein the functional unit is configured to perform the operation on two operands, wherein the second operand is provided by a source other than the first and second memory banks in column 9, lines 29-38.

10. As per claim 12, Saito discloses a functional unit configured to perform an operation on one or more block operands; an accumulator memory comprising a first

memory bank having a first interface and a second memory bank having a second interface, wherein the first and second interfaces are independent of each other; and a control unit configured to receive commands to perform the operation, wherein each command to perform the operation instructs the control unit to perform the operation on an operand identified by a first address in the accumulator memory and to store a result of the operation to a second address in the accumulator memory; wherein in response to every command to perform the operation that the control unit receives, the control unit is configured to provide the operand from one of the first and second memory banks to the functional unit and to map the second address to a location in the other one of the first and second memory banks so that the result of the operation is always stored in a different memory bank than the operand is stored in column 9, lines 1-51. The functional unit is the XOR gate (35), the accumulator memory is RAM(p1) and RAM(p2), and the control unit is the control circuit (34).

Saito discloses wherein the functional unit is configured to perform the operation on two operands, wherein one of the operands is provided by either the first or the second memory bank and the other operand is provided by a source other than the first and second memory banks in column 9, lines 29-38.

Saito fails to explicitly state the source and the accumulator memory each comprise a same type and speed of memory.

Bains discloses this limitation in column 7, lines 35-46.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source and the accumulator memory each

comprise a same type and speed of memory. A person of ordinary skill in the art would have been motivated to have the source and the accumulator memory each comprise a same type and speed of memory because the data can be accessed at the same rate so as not to reduce the overall performance of the computer system. Bains discloses this in column 1, lines 11-17.

11. As per claim 13, Saito discloses wherein the first and second addresses are the same in column 9, lines 52-65.

12. As per claim 14, Saito discloses wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller in column 8, lines 11-41.

13. As per claim 20, Saito discloses wherein the operation has a duration extending from when the operation is initiated to when the operation completes, and wherein for the duration of the operation that is performed on a first operand, the first memory bank is in a providing mode and the second memory bank is in a storing mode in column 9, lines 21-51.

14. As per claim 21, Saito discloses receiving a first command to perform an operation on a first operand identified by a first address and to store a first result of the operation to the first address; and in response to said receiving a first command: providing the first operand from a first memory bank in an accumulator memory via a first interface; performing the operation on the first operand; and storing the first result of the operation in a second memory bank in the accumulator memory via a second interface, wherein the first and second interface are independent of each other in

column 9, lines 1-51. The functional unit is the XOR gate (35), the accumulator memory is RAM(p1) and RAM(p2), and the control unit is the control circuit (34).

Saito discloses wherein said performing the operation on the first operand comprises performing the operation on both the first operand and another operand wherein the other operand is provided by a source other than the first and second memory banks in column 9, lines 29-38.

Saito fails to explicitly state the source memory and the accumulator memory each comprise a same type and speed of memory.

Bains discloses this limitation in column 7, lines 35-46.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source and the accumulator memory each comprise a same type and speed of memory. A person of ordinary skill in the art would have been motivated to have the source and the accumulator memory each comprise a same type and speed of memory because the data can be accessed at the same rate so as not to reduce the overall performance of the computer system. Bains discloses this in column 1, lines 11-17.

15. As per claim 22, Saito discloses causing the second memory bank to provide a second operand in response to receiving another command that identifies the second operand using the first address after said storing the first result of the operation in the second memory bank in column 9, lines 21-51.

16. As per claim 23, Saito discloses receiving a second command to perform the operation on a second operand identified by the first address and to store a second

result of the operation to the first address; and in response to said receiving a second command: providing the second operand from the second memory bank via the second interface; performing the operation on the second operand; and storing the second result in the first memory bank via the first interface in column 9, lines 21-51.

17. As per claim 24, Saito discloses causing the first memory bank to provide a third operand in response to receiving another command that identifies the third operand using the first address after said storing the second result of the operation in the first memory bank in column 9, lines 21-51.

18. As per claim 25, Saito discloses wherein the operation has a duration extending from when the operation is initiated to when the operation completes, and wherein for the duration of the operation that is performed on the first operand, the first memory bank is in a providing mode and the second memory bank is in a storing mode in column 9, lines 21-51.

19. As per claim 26, Saito discloses wherein the operation comprises a parity calculation, and wherein the first command is issued by a storage system controller in column 8, lines 11-41.

20. As per claim 32, Saito discloses receiving one or more commands to perform an operation on an operand identified by a first address in an accumulator memory and to store a result of the operation to a second address in the accumulator memory, wherein the accumulator memory comprises two independently interfaced memory banks; and in response to receiving each of the one or more commands: providing the operand from one of memory banks in the accumulator memory; performing the operation on the

operand; and mapping the second address to a new address in the other one of the memory banks in the accumulator memory so that the result of the operation is always stored in a different memory bank than the operand is stored in column 9, lines 1-51. The functional unit is the XOR gate (35), the accumulator memory is RAM(p1) and RAM(p2), and the control unit is the control circuit (34).

Saito discloses wherein said performing the operation on the operand comprises performing the operation on a first operand provided by the accumulator memory and another operand provided by a source other than the accumulator memory in column 9, lines 29-38.

21. As per claim 33, Saito discloses wherein the first and second addresses are the same in column 9, lines 52-65.

22. As per claim 34, Saito discloses wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller in column 8, lines 11-41.

23. Claims 7,17,29,37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of Bains in further view of Elliott et al. (USPN 5392425A). As per claim 7, Saito and Bains fail to explicitly state the control unit is configured to restart the operation in response to an error occurring by providing the first operand from the first memory bank again and by storing the result of the restarted operation in the second memory bank.

Elliott et al. discloses this limitation in column 3, lines 50-54 and column 7, lines 37-50.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the control unit to restart the operation in response to an error. A person of ordinary skill in the art would have been motivated to have the control unit to restart the operation in response to an error because retrying the parity calculation helps to determine if the parity error is transient or if something is wrong with the computer system.

24. As per claim 17, Saito and Bains fail to explicitly state during the performance of the operation initiated by receiving one of the commands, the control unit is configured to restart the operation in response to an error occurring by providing the operand from the one of the first and second memory banks again.

Elliott et al. discloses this limitation in column 3, lines 50-54 and column 7, lines 37-50.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the control unit to restart the operation in response to an error. A person of ordinary skill in the art would have been motivated to have the control unit to restart the operation in response to an error because retrying the parity calculation helps to determine if the parity error is transient or if something is wrong with the computer system.

25. As per claim 29, Saito and Bains fail to explicitly state restarting said performing the operation on the first operand in response to an error occurring, wherein said restarting comprises providing the first operand from the first memory bank again and storing the result of the restarted operation in the second memory bank.

Elliott et al. discloses this limitation in column 3, lines 50-54 and column 7, lines 37-50.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the control unit to restart the operation in response to an error. A person of ordinary skill in the art would have been motivated to have the control unit to restart the operation in response to an error because retrying the parity calculation helps to determine if the parity error is transient or if something is wrong with the computer system.

26. As per claim 37, Saito and Bains fail to explicitly state restarting said performing the operation on a first operand in response to an error occurring, wherein said restarting comprises providing the first operand from a first memory bank again and storing the result of the restarted operation in a second memory bank.

Elliott et al. discloses this limitation in column 3, lines 50-54 and column 7, lines 37-50.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the control unit to restart the operation in response to an error. A person of ordinary skill in the art would have been motivated to have the control unit to restart the operation in response to an error because retrying the parity calculation helps to determine if the parity error is transient or if something is wrong with the computer system.

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Response to Arguments

27. Applicant's arguments filed 08/30/2004 have been fully considered but they are not persuasive. Applicant argues that 'The combination of Saito and Bains actually teaches away from the operands being provided by the same type of memory, given that Bains expressly teaches the desirability of the use of different memory types and Saito requires that its memory 12 be a dual-port memory as opposed to the single port memories 30 and 31.'

Examiner respectfully disagrees with Applicant. Bains teaches that you can have memories of the same type and speed. Examiner points out for the 103 rejection made for this limitation in column 7, lines 35-46 of how memories of the same type and speed can be accessed. Saito provides a dual-port DRAM memory. The difference between a dual port memory and a single port memory as given by National Instruments is a dual-port memory is memory that can be simultaneously accessed by more than one controller or processor; therefore, this type of memory has added components which allows more than one piece of hardware to access. The type of dual-port memory discussed in Saito is a DRAM memory. As noted by Webster's Online Dictionary, a not so common type of Ram is a Dual-ported RAM. Therefore, although a dual-port DRAM was used it would be obvious to also have a dual-port RAM, so that this type of memory can be consistent with the other two RAM memories associated with the parity circuit of Saito.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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